IN THE SPECIFICATION

Please amend the Abstract of the specification as follows:

A method to handle data dependencies in a pipelined computer system is disclosed. The method includes allocating a plurality of registers, enabling execution of computer instructions concurrently by using the plurality of registers, and tracking and reducing data dependencies in the computer instructions by correlating a busy condition of a computer instruction to each register.

Please amend paragraph 21 on page 10 of the specification as follows:

[0021] One configuration of a predicate register file 100 with an associated scoreboard 102 is illustrated in FIG. 1 in accordance with an embodiment of the present invention. The scoreboard 102 has a busy bit for each register. A predicate-reading instruction 200 then checks the busy bit for its source predicate, as shown in FIG. 2. This may happen either before or after the ~~execute~~ execution as long as instructions reading the same predicate register 202 check the bit in-order. If the busy bit is null, the instruction 200 may safely copy and use the value in the predicate register 202. Otherwise, the instruction 200 must stall until the result is bypassed.